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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/301,853	04/29/1999	KAZUHISA OHBUCHI	FUJS-16.073	6159

7590 12/27/2002

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EXAMINER
LAMARRE, GUY J

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)	
09/301,853	OHBUCHI ET AL.	
Examiner	**Art Unit**	
Guy J. Lamarre, P.E.	2133	

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *08 November 2002* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *16* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

0. A request for continued examination (paper # 14), under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's pre-amendment (paper # 15), filed on *08 November 2002,* has been entered.

Applicant's petition of 3-month extension of time (paper # 13), filed on *08 November 2002*, has been granted.

The IDS (paper # 16), filed on *05 December 2002, has been entered and considered by the Examiner.*

Applicant's supplemental amendment (paper # 17), filed on *05 December 2002,* has been entered. This office action is in response to Applicants' preliminary and supplemental amendments.

0.1 Claims 1-4, 10, 14, 17-20, 23-24, 31-32, 35-36 and 43-53 are amended. Claims 1-53 remain pending.

0.2 The rejections and objections of record are withdrawn in response to Applicants' amendment, filed on *08 November 2002 and 05 December 2002*.

0.3 Claims 1-53 are **now** rejected under 35 U.S.C. 103(a) as being unpatentable as follows.

Response to Arguments

0.4 Applicants' arguments, filed *08 November 2002 and* 05 *December 2002, along with the entire disclosure* have been fully considered.

It is not clear to the examiner where the invention is claimed. Specifically Fig. 6 depicts original data in a matrix or M1, Fig. 7 depicts column permutation of said matrix M1 resulting in matrix M2, Fig. 8 depicts row permutation of matrix M2 resulting in matrix M3, and Fig. 9 depicts transformation of matrix M3 into 1X384 matrix, or matrix M4, by appending the columns of matrix M3 so as to result in A1..A24P1..P24,...O1..O24H1..H24. Therefore, four matrices are used.

However such data rearrangement is not claimed. For example, Claim 1 recites that there are only three matrices: a first matrix or M1 for original data, a second matrix M2 for row interchanging and column interchanging, and a third matrix or what corresponds to matrix M4 for outputting serial permuted data. Therefore, matrix M3 is not formed.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first and second paragraphs of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
>
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1.1. **Claims 1-53** are rejected under **35 USC § 112** first Paragraph for failing to describe in the specification how to manipulate original data in a single matrix by simultaneously interchanging rows and columns using said single matrix without losing track of the location of said original data.

1.2 **Claims** 1-53 are rejected under 35 USC § 112 SECOND PARAGRAPH for failing to particularly point out and distinctly define the subject matter which the applicant regards as his invention. It is not clear to the examiner how the permuting of columns is operatively performed. Specifically, it is not clear to the examiner how the rows and columns of a matrix are

interchanged to effect data shuffling without causing confusion as to the location of said original data subsequent to data permutation.

Claim Rejections - 35 USC ' 103

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

2.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.1 **Claims 1-53** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Lin et al.** (US Patent No. 5,068,878; February 6, 1990).

As per Claims 1, 2, 3, 10, 17-24, 31-32, 35-36, 43, 46 and 49, Admitted prior art substantially discloses the procedure for the claimed interleaving means (or reverse operation) comprising the steps of: arranging data to be transmitted in a matrix; and rearranging or spreading by interchanging rows of the matrix according to a predetermined order, each row representing a set of data pieces of said data and rearranging or spreading by interchanging columns of the matrix according to a predetermined order, each column representing a set of data pieces of said data; and outputting said rearranged data in time series. {See **Admitted prior art,** Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein rearranging or spreading means are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted or spread row or column-wise in a random or predetermined fashion or order (Examiner notes that even though the data interleaving is effected in a random fashion, said

predetermined fashion or order interleaving is known by the de-interleaver, de-interleaver that will use such knowledge to operate on interleaved data so as to recover the original data. Therefore, there is a predetermination in the order in which the interleaver arranges the original data.), and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving or de-spreading) to recover said data; and control means to perform data shuffling and re-ordering; means to perform error detection and correction (page 3 line 25); means for data communication or transmission via radio or antenna means (page 1 line 17).} **Not specifically described** in detail in **Admitted prior art** is the step whereby random or predetermined fashion or order of rearranging data by columns or rows is performed in time series or sequentially.

However such approach is well known. For example, **Lin et al.,** in an analogous art, discloses algorithms wherein such techniques are described. {See **Lin et al.,** Id., Abstract.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of the **Admitted prior art** by including therein a mathematical method as taught by **Lin et al.,** because such modification would provide the procedure disclosed in the **Admitted prior art** with a technique whereby the "*[The] controller 100 then allows the flow of data from the data source 101 to continue. Referring to FIG. 3, it will be appreciated that the* ***resynchronization signals*** *134, 136, 138, 140, ... 154 are thereby recordable on the tape 77* ***in a pseudo-random fashion relative to the interleave block boundaries****. It will be noted that the resynchronization signals 134-154 are inserted in addition to the recorded data bytes; the flow of data being momentarily interrupted to accommodate the recording of the resynchronization signals.*" {See **Lin et al.,** col. 7 line 17-et seq.}

As per Claims 4, 11, 25-26, 44-45, 47-48, 50-53, Lin et al. discloses the procedure for the claimed interleaving means, wherein said control unit comprises a write control unit for

generating a write address to be used to write said data to be transmitted in said storing unit with said data to be transmitted arranged in a matrix and rearranged or spread by interchanging rows of the matrix according to a predetermined order, each row representing a set of data pieces of said data and by interchanging columns of the matrix according to a predetermined order, each column representing a set of data pieces of said data, and for writing said data to be transmitted in said storing unit, and said control unit reads said data to be transmitted stored in said first storing unit in the order of addresses. {See **Lin et al.,** col. 5 line 67-et seq., for data writing means effected by *"controller 100 which now sequences the changeover so that RAM 96 is read out and the RAM 96' is written into, as previously mentioned (FIG. 4).* }

As per Claims 5, 12, 27-30, Lin et al. discloses the procedure for the claimed interleaving means, wherein said write control unit comprises a column number generating unit for randomly generating column numbers and a row number generating unit for randomly generating row numbers, and said first write control unit writes said data to be transmitted in said first storing unit with numbers generated by said column number generating unit and said row number generating unit as said write address to write said data to be transmitted in said first storing unit.. {See **Lin et al.,** col. 5 line 67-et seq., for data writing means effected by *"controller 100 which now sequences the changeover so that RAM 96 is **read out** and the RAM **96' is written into**, as previously mentioned (FIG. 4).* } Also refer to **Admitted prior art,** Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a random fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.}

As per Claims 6, 13, 39-42, Lin et al. discloses the procedure for the claimed interleaving apparatus according to claim 5(12), 2 wherein each of said column number generating unit and said row number generating unit is configured with a memory for holding numbers used as addresses in a predetermined order {See **Lin et al.** col. 6 lines 17- et seq., wherein for address generation means via counter 108.}

As per Claims 7, 14, 33-34, Lin et al. discloses the procedure for the claimed interleaving apparatus according to claim 3(10), wherein said first control unit writes said data to be transmitted in said first storing unit in the order of addresses, and said first control unit comprises a first read controlling unit for generating a read address to be used to read said data to be transmitted from said first storing unit with said data to be transmitted stored in said first storing unit arranged in a matrix and at least either columns or rows of said data to be transmitted randomly rearranged to read said data to be transmitted. {See **Lin et al.,** col. 5 line 67-et seq., for data writing means effected by *"controller 100 which now sequences the changeover so that RAM 96 is **read out** and the RAM **96' is written into**, as previously mentioned (FIG. 4).* } Also refer to **Admitted prior art,** Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a random fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.}

As per Claims 8, 15, 37-38, Lin et al. discloses the procedure for the claimed interleaving apparatus according to claim 7 (14), wherein said first read control unit comprises a column number generating unit for randomly generating column numbers and a row number generating unit for randomly generating row numbers, and said first read control unit reads said

data to be transmitted from said first storing unit with numbers generated by said column number generating unit and said row number generating unit as said read address. {See **Lin et al.,** col. 5 line 67-et seq., for data writing means effected by *"controller 100 which now sequences the changeover so that RAM 96 is **read out** and the RAM **96' is written into**, as previously mentioned (FIG. 4).* } Also refer to **Admitted prior art,** Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a random fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.}

As per Claims 9, 16, Lin et al. discloses the procedure for the claimed The interleaving apparatus according to claim 8(15), wherein each of said column number generating unit and said row number generating unit is configured with a memory for holding numbers used as addresses in a predetermined order {See **Lin et al.,** col. 7 lines 35- et seq., wherein predetermined order means is provided for permuting information.}

2.2 Claims 1, 2, 3, 10, 17-24, 31-32, 35-36, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Azuma et al.** (US Patent No. 4959863; June 2, 1988).

As per Claims 1, 2, 3, 10, 17-24, 31-32, 35-36, 43, 46 and 49, Admitted prior art substantially discloses the procedure for the claimed interleaving means (or reverse operation) comprising the steps of: arranging data to be transmitted in a matrix; and rearranging or spreading by interchanging rows of the matrix according to a predetermined order, each row representing a set of data pieces of said data and rearranging or spreading by interchanging columns of the matrix according to a predetermined order, each column representing a set of data pieces of said data; and outputting said rearranged data in time series. {See **Admitted prior art,**

Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein rearranging or spreading means are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted or spread row or column-wise in a random or predetermined fashion or order (Examiner notes that even though the data interleaving is effected in a random fashion, said predetermined fashion or order interleaving is known by the de-interleaver, de-interleaver that will use such knowledge to operate on interleaved data so as to recover the original data. Therefore, there is a predetermination in the order in which the interleaver arranges the original data.), and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving or de-spreading) to recover said data; and control means to perform data shuffling and re-ordering; means to perform error detection and correction (page 3 line 25); means for data communication or transmission via radio or antenna means (page 1 line 17).} **Not specifically described** in detail in **Admitted prior art** is the step whereby random or predetermined fashion or order of rearranging data by columns or rows is performed in time series or sequentially.

However such approach is well known. For example, **Azuma et al.,** in an analogous art, discloses algorithms wherein such techniques are described. {See **Azuma et al.,** Id., Abstract.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of the **Admitted prior art** by including therein a random or predetermined fashion or order permutation method as taught by **Azuma et al.,** because such modification would provide the procedure disclosed in the **Admitted prior art** with a technique whereby the "[*The] decimated signal sequence (signal vector) Y.sup.i' (Z.sup.16) is permutated by a multiplication by the permutation matrix [T] of 8.times.8. In this case, the row element of the permutation matrix is 0 or 1 (the sum being 1), and element of this matrix is 0 or 1 (the sum being 1). The permutation matrix is a fixed permutation if constant*

with time, and ***a variable permutation if variable****. In the scramble processing,* ***the rows of this matrix are permutated at random****, and the number of combinations is usually n! for an n.times.n matrix.*" {See **Azuma et al.,** col. 10 line 59-et seq.}

2.3 Claims 1, 2, 3, 10, 17-24, 31-32, 35-36, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Yamaguchi et al.** ("Turbo Code", a new coding system approaching theoretical Shannon limits, is born in France; NIKKEI ELECTRONICS, July 13, 1988).

As per Claims 1, 2, 3, 10, 17-24, 31-32, 35-36, 43, 46 and 49, Admitted prior art substantially discloses the procedure for the claimed interleaving means (or reverse operation) comprising the steps of: arranging data to be transmitted in a matrix; and rearranging or spreading by interchanging rows of the matrix according to a predetermined order, each row representing a set of data pieces of said data and rearranging or spreading by interchanging columns of the matrix according to a predetermined order, each column representing a set of data pieces of said data; and outputting said rearranged data in time series. {See **Admitted prior art,** Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein rearranging or spreading means are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted or spread row or column-wise in a random or predetermined fashion or order (Examiner notes that even though the data interleaving is effected in a random fashion, said predetermined fashion or order interleaving is known by the de-interleaver, de-interleaver that will use such knowledge to operate on interleaved data so as to recover the original data. Therefore, there is a predetermination in the order in which the interleaver arranges the original data.), and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving or de-spreading) to recover said data; and control means to perform data shuffling and re-ordering; means to perform error detection and correction (page 3 line 25); means for data communication or transmission via radio or antenna means

(page 1 line 17).} **Not specifically described** in detail in **Admitted prior art** is the step whereby random or predetermined fashion or order of rearranging data by columns or rows is performed in time series or sequentially.

However such approach is well known. For example, **Yamaguchi et al.,** in an analogous art, discloses algorithms wherein such techniques are described. {See **Yamaguchi et al.,** Id., Excerpt translation : page 1 first and second paras. last line.} **Therefore,** it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of the **Admitted prior art** by including therein a random or predetermined fashion or order permutation method as taught by **Yamaguchi et al.,** because such modification would provide the procedure disclosed in the **Admitted prior art** with a technique whereby it is possible to ***greatly change the characteristics of the turbo codes,*** or ***to improve weight distribution of said codes*** {See **Yamaguchi et al.,** Excerpt translation : page 1 last para first sentence.}

2.4 Claims 1, 2, 3, 10, 17-24, 31-32, 35-36, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Karasawa et al.** (US Patent No. 5,204,981; Mar. 1, 1991).

As per Claims 1, 2, 3, 10, 17-24, 31-32, 35-36, 43, 46 and 49, Admitted prior art substantially discloses the procedure for the claimed interleaving means (or reverse operation) comprising the steps of: arranging data to be transmitted in a matrix; and rearranging or spreading by interchanging rows of the matrix according to a predetermined order, each row representing a set of data pieces of said data and rearranging or spreading by interchanging columns of the matrix according to a predetermined order, each column representing a set of data pieces of said data; and outputting said rearranged data in time series. {See **Admitted prior art,** Figs. 22-24, and page 1 line 17 – page 8 line 5, in passim, wherein rearranging or spreading means are described, e.g. data is acquired, stored or arranged in matrix or array form,

subsequently permuted or spread row or column-wise in a random or predetermined fashion or order (Examiner notes that even though the data interleaving is effected in a random fashion, said predetermined fashion or order interleaving is known by the de-interleaver, de-interleaver that will use such knowledge to operate on interleaved data so as to recover the original data. Therefore, there is a predetermination in the order in which the interleaver arranges the original data.), and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving or de-spreading) to recover said data; and control means to perform data shuffling and re-ordering; means to perform error detection and correction (page 3 line 25); means for data communication or transmission via radio or antenna means (page 1 line 17).} **Not specifically described** in detail in **Admitted prior art** is the step whereby random or predetermined fashion or order of rearranging data by columns or rows is performed in time series or sequentially.

However such approach is well known. For example, **Karasawa et al.,** in an analogous art, discloses algorithms wherein such techniques are described. {See **Karasawa et al.,** Id., Fig. 9 and Abstract: last line.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of the **Admitted prior art** by including therein a permutation method as taught by **Karasawa et al.,** because such modification would provide the procedure disclosed in the **Admitted prior art** with a technique whereby it is possible to design "***An interleaver 10*** which ***stores a fixed amount of signal sequence output from the FEC coder 9 and outputs it in a time series different from that of the input. That is, the interleaver 10 stores a fixed amount of data in a predetermined two-dimensional memory and provides the output, for example, in a column order if the input was applied in a row order.***" {See **Karasawa et al.,** col. 3 lines 5-et seq.}

2.5 Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable **Karasawa et al.** (US Patent No. 5,204,981; Mar. 1, 1991) in

view of **Yamaguchi et al.** ("Turbo Code", a new coding system approaching theoretical Shannon limits, is born in France; NIKKEI ELECTRONICS, July 13, 1988) in further view of **de Almeida et al.** (Two-Dimensional Interleaving Using the Set Partitioning Technique; IEEE, Aug. 1994).

As per Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49, Karasawa substantially discloses the procedure for the claimed interleaving means (or reverse operation) comprising the steps of: arranging data to be transmitted in a matrix; and rearranging or spreading by interchanging rows of the matrix according to a predetermined order, each row representing a set of data pieces of said data and rearranging or spreading by interchanging columns of the matrix according to a predetermined order, each column representing a set of data pieces of said data; and outputting said rearranged data in time series. {See **Karasawa** , Fig. 9, Abstract: last line and col. 3 lines 5-et esq., in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a some fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.} **Not specifically described** in detail in **Karasawa** is the step whereby random rearranging by either columns or rows of data is effected.

However such approach is well known. For example, **Yamaguchi et al.,** in an analogous art, discloses algorithms wherein such techniques are described. {See **Yamaguchi et al.,** Id., Excerpt translation : page 1 first and second paras. last line.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Karasawa** by including therein a random permutation method as taught by **Yamaguchi et al.,** because such modification would provide the procedure disclosed in **Karasawa with** a technique whereby it is possible to ***greatly change the characteristics of the***

turbo codes, or ***to improve weight distribution of said codes*** {See **Yamaguchi et al.,** Excerpt translation: page 1 last para first sentence.}

While Karasawa and **Yamaguchi et al** substantially disclose the procedure for the claimed invention, **they fail to specifically describe** in detail the concept whereby random rearrangement of data is effected by exchanging data units at least between rows and columns.

However, such technique is well known in data processing systems, e.g., **de Almeida et al.,** in an analogous art, discloses an algorithm wherein such random rearrangement means is depicted. {See **de Almeida et al.,** Id., Example 1, Fig.1 and Table 1.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Karasawa** and **Yamaguchi et al** by including therein the technique as disclosed by **de Almeida et al**. because such modification would provide the procedure of **Karasawa** and **Yamaguchi et al** with a method whereby " *simple random-error-correcting codes can be used to correct clusters of errors, instead of the more complex burst-error-correcting codes.* " {See **de Almeida et al. Id.,** SUMMARY: para. 1 last sentence, and col. 1 penultimate para.}

2.6 Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable **Karasawa et al.** (US Patent No. 5,204,981; Mar. 1, 1991) in view of **Azuma et al.** (US Patent No. 4959863; June 2, 1988) in further view of **de Almeida et al.** (Two-Dimensional Interleaving Using the Set Partitioning Technique; IEEE, Aug. 1994).

As per Claims 1, 2, 3, 10, 17-20, 23-24, 31-32, 35-36, 43, 46 and 49, Karasawa substantially discloses the procedure for the claimed interleaving means (or reverse operation) comprising the steps of: arranging data to be transmitted in a matrix; and rearranging or spreading by interchanging rows of the matrix according to a predetermined order, each row representing a set of data pieces of said data and rearranging or spreading by interchanging columns of the matrix according to a predetermined order, each column representing a set of data pieces of said data; and outputting said rearranged data in time series. {See **Karasawa** , Fig. 9,

Abstract: last line and col. 3 lines 5-et esq., in passim, wherein apparatus and method are described, e.g. data is acquired, stored or arranged in matrix or array form, subsequently permuted row or column-wise in a some fashion, and said permutation or interleaving operation being timed or synchronized via a clock; means to reverse data ordering (de-interleaving) to recover said data; and control means to perform data shuffling and re-ordering.} **Not specifically described** in detail in **Karasawa** is the step whereby random or variable rearranging by either columns or rows of data is effected.

However such approach is well known. For example, **Azuma et al.,** in an analogous art, discloses algorithms wherein such techniques are described. {See **Azuma et al.,** Id., Abstract.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Karasawa** by including therein a mathematical method as taught by **Azuma et al.,** because such modification would provide the procedure disclosed in **Karasawa** with a technique whereby the "[*The] decimated signal sequence (signal vector) Y.sup.i' (Z.sup.16) is permutated by a multiplication by the permutation matrix [T] of 8.times.8. In this case, the row element of the permutation matrix is 0 or 1 (the sum being 1), and element of this matrix is 0 or 1 (the sum being 1). The permutation matrix is a fixed permutation if constant with time, and* ***a variable permutation if variable****. In the scramble processing,* ***the rows of this matrix are permutated at random****, and the number of combinations is usually n! for an n.times.n matrix.*" {See **Azuma et al.,** col. 10 line 59-et seq.}

While Karasawa and **Azuma et al** substantially disclose the procedure for the claimed invention, **they fail to specifically describe** in detail the concept whereby random rearrangement of data is effected by exchanging data units at least between rows and columns.

However, such technique is well known in data processing systems, e.g., **de Almeida et al.,** in an analogous art, discloses an algorithm wherein such random rearrangement means is depicted. {See **de Almeida et al.,** Id., Example 1, Fig.1 and Table 1.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Karasawa** and **Azuma et al** by including therein the technique as disclosed by **de Almeida et al**. because such modification would provide the procedure of **Karasawa** and **Azuma et al** with a method whereby " *simple random-error-correcting codes can be used to correct clusters of errors, instead of the more complex burst-error-correcting codes.* " {See **de Almeida et al. Id.,** SUMMARY: para. 1 last sentence, and col. 1 penultimate para.}

Claim Objections

3. The listed claims are objected to because of the following informalities: **C**laim 47 line 7 reads '...[interchanging...' and **C**laim 48 line 8 reads '...]interchanging...' Appropriate correction is required.

Drawings

4. Drawings are objected to because Figs. 8A and 8B, referred to on page 19 line 8, are not seen. Appropriate correction to drawings as required by form PTO 948 shall be made in response to current Office action as per 37 CFR 1.85(a).

Specification

5. The disclosure is objected to as non-compliant with 37 CFR 1.74 because description of Fig. 8, as depicted, does not include anything related to Figs. 8A and 8B, as referred to on page 19 line 8. Specification to be amended accordingly. Appropriate correction is required.

Conclusion

6. The prior art made of record and relied upon is considered to applicant's disclosure. The references are cited in Form PTO-892 for the Applicant's review and comments, in particular **Schreiber** and **Wootton et al.** These two references relate to data arranged in a matrix undergoing random or pseudo-random interleaving by rows and columns.

6.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to:

(703) 746-7238, (for After-Final communications),

(703) 746-7239, (for formal communications intended for entry),

(703) 746-5463 (for informal or draft communications, please label "PROPOSED" or "DRAFT").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Guy J. Lamarre, P.E.

Guy J. Lamarre

Patent Examiner

12/12/02